8.6 TCAM for IP-Address Lookup Using Tree-style AND-type Match Lines and Segmented Search Lines

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High speed and low energy remain two challenges for CAM design. In this paper, a tree-style AND-type match line and a segmented search-line schemes that cooperatively top the constituent TCAM, are presented. These TCAMs are fast and energy efficient for applications like IP-address lookup in a network router. The realized 256×128b TCAM macro achieves 26% speed improvement and 39% energy reduction, as compared to state-of-the-art binary CAM (BiCAM) [1].

The concept of AND-type match line first appeared in [1]. For a 256×128b CAM, the original realization comprised of two branches of 11-stage series-cascaded pseudo-footless clock-and-data precharged dynamic (*PF-CDPD*) AND-type match lines. The final match result is obtained via a 2-input static AND gate (Fig. 8.6.1, (a)). It is demonstrated that this scheme not only improved the search speed, but also reduced the power consumption.

For further speed-up of the *PF-CDPD* AND scheme, three versions of tree-style match lines are investigated. The first one (Fig. 8.6.1, (b)) has the same logic depth as the original design. Yet for each stage except the first, the AND function is performed by a separated 6-input dynamic AND gate. Since these separate gates are not on the critical path, the match speed is improved. However, power consumption is increased due to the requirement of a larger clock driver. The second one (Fig. 8.6.1, (c)) adopts a three-level tree structure, where the longest path is reduced to 5 *PF-CDPD* AND gates plus one 6-input static AND gate. Although this scheme does not incur extra power consumption like the previous one, the speed improvement is quite limited because 1) the 6-input static AND gate is slow; and 2) the interconnections among the dynamic gates induce much RC delay. In lieu of the pros and cons of the previous two approaches, a two-level tree structure (Fig. 8.6.1, (d)) is proposed to improve the speed and power indices. It can be seen that there is no extra power consumption as in Fig. 8.6.1(a), and the speed of critical path (now contains 6 *PF-CDPD* AND gates plus one 4-input static AND gate) is higher than Fig. 8.6.1(c) due to the large speed difference between the 6-input and 4-input static AND gates and reduced interconnect RC delay.

Because the entire match line should be arranged in a single row, the layout of the two-level tree-style match line deserves further attention. A straightforward layout, shown in the upper part of Fig. 8.6.2, results in very long interconnections and adds significant RC delays to the search operation. Hence, the leap-frog interconnection with minimal hops is used, as shown in the lower part of Fig. 8.6.2, to shorten the interconnection among gates and maintain the search speed.

For power consumption, a TCAM consumes power mainly in 3 parts: clock and control, match line, and search line. Thanks to the advancement of match-line design techniques, the power consumption of the former two has been greatly reduced. This can be seen from the works of the past three years [2, 3, 1], where the power consumption for search lines occupies about 54%, 71%, and 82% of the total power, respectively. To tackle the power consumption problem on search lines, pipelining and hierarchical search lines are used in [4]. However, the area and power overhead caused by the pipeline flip-flops and the clock driver diminishes the usefulness of the approach.

The problem is addressed by taking advantage of application features of TCAM. For example, in IP-address lookup in a network router, the mask (don't care) bits are located in a progressive pattern shown in cells marked with "*x*" in the left part of Fig. 8.6.3 [5]. Since these "*x*" cells do nothing but passing the matching signal, they do not have to be involved with the search line. This property, when combined with the progressive layout pattern, indicates that search lines behind the "*x*" cells can be turned off to save energy. The idea leads to the segmented search line designs shown in the right part of Fig. 8.6.3. The circuit containing an SC and two ternary cells (T cells) is shown in Fig. 8.6.4. The SC is composed of a dummy cell and a path-control switch. The WL for the upper T cell is also for the dummy cell. When writing an *x* into the upper T cell, both bit and bit bar lines are raised to high. In this case, the output *q* of the dummy cell gets a "low" to cut off the search path, and the upper segment of the search line (SBL_u) will be pulled down to ground. In other words, when the ternary cell above the segmentation cell (SC) stores an *x*, the segmentation cell will automatically block the search signal from propagating forward and save the energy.

A test chip is designed for a 0.18µm 1.8V 256×128b TCAM macro with two segmentation rows, one at the quarter and the other at the half of the search line. The internal clock signal has a 50% duty cycle, and flip-flops are used to capture the matching results. As shown in Fig. 8.6.5, the search time can be calculated as $t_{search} = 0.5 \times t_{cycle} - t_{su}$, where t_{cycle} is the measured clock cycle time, and t_{su} is the simulated set-up time of the flip-flop (5.2ps). The proposed TCAM macro achieves the fastest reported search time of 1.56ns. 4×32b LFSRs and a mask-bit control circuit are used to get routing-table-like test patterns similar to that shown in Fig. 8.6.3. With these test patterns, the proposed TCAM macro achieves the energy consumption of 1.42fJ/b/search at 1.8V, as illustrated in Fig. 8.6.6. The area overhead due to segmentation cells is 3.3%. Performance comparisons are given as follows. For the same CMOS technology, the proposed design is 55% better in speed and 51% less in energy compared to the TCAM in [4]. It is also 26% better in speed and 39% less in energy compared to the BiCAM in [1].

A similar 256×128b TCAM macro is also designed in a 0.13µm 1.2V CMOS technology. Post-layout simulation shows that the 0.13µm TCAM achieves 1.10ns search time with 0.348fJ/b/search energy index, as compared to 2.2ns and 0.7fJ/b/search reported in the state-of-the-art multi-bank 0.1µm 1.2V TCAM [3] that adopted NOR-type bank-selection circuit and NAND-type match-lines. Fig. 8.6.7 shows the chip micrograph.

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References:
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[4] K. Pagiamtzis, et al., "A Low-Power Content-Addressable Memory (CAM) Using Pipelined Hierarchical Search Scheme," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1512-1519, Sept., 2004.
[5] BGP table statistics, (web: http://bgp.potaroo.net), Dec., 3, 2004.

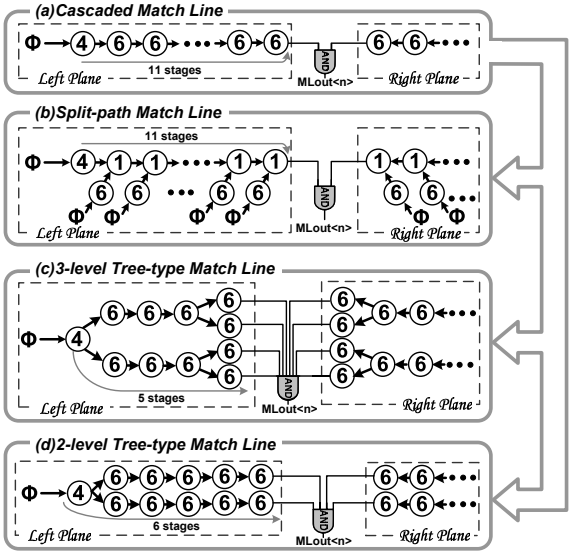

Figure 8.6.1: Match line architectures.

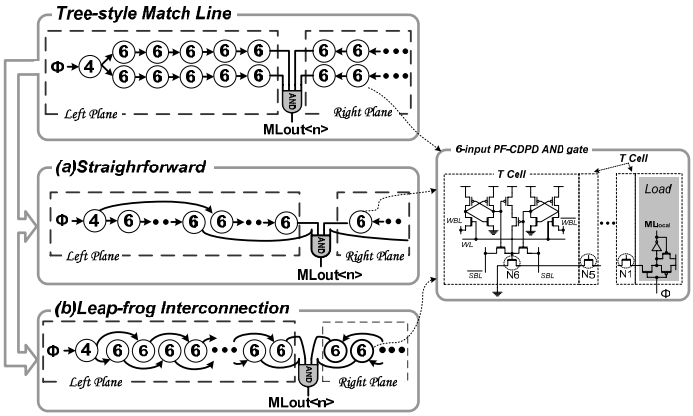

Figure 8.6.2: Implementation of tree-style match line.

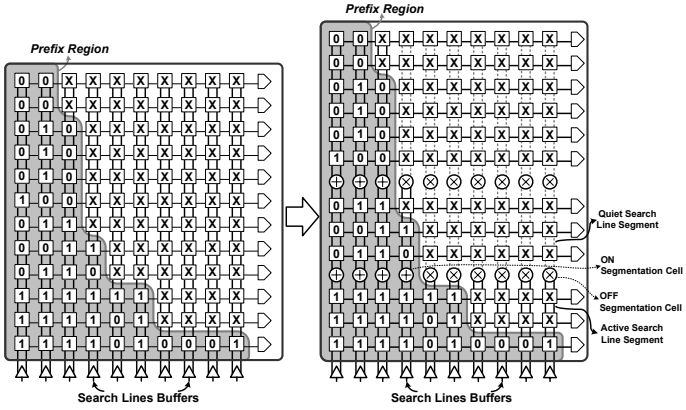

Figure 8.6.3: Concept of segmented search lines.

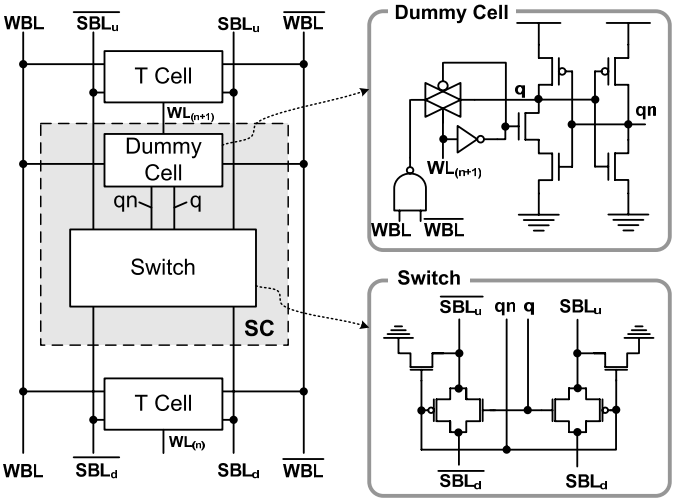

Figure 8.6.4: Segmentation Cell Design.

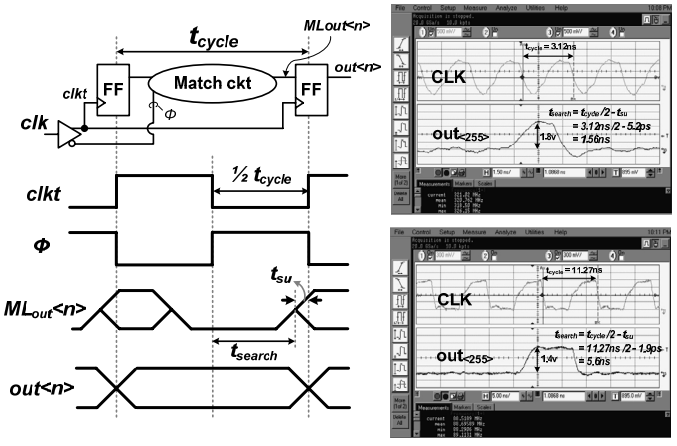

Figure 8.6.5: Measurement setup and results.

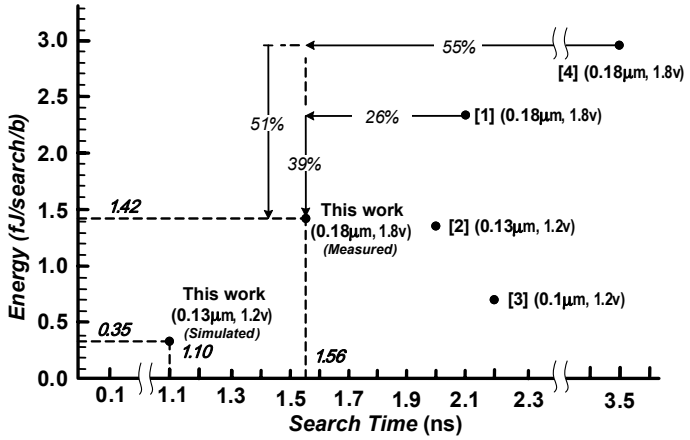

Figure 8.6.6: Performance comparison.

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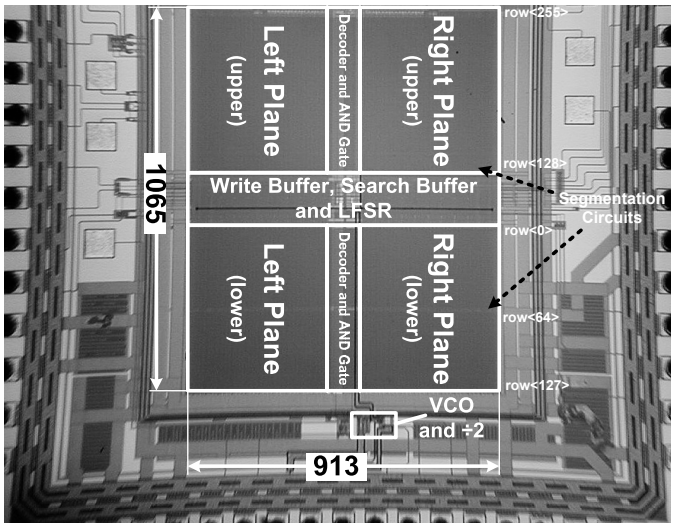

Figure 8.6.7: Chip micrograph.

